

UNITED STATES PATENT APPLICATION

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FOR

**ISOTROPIC DRY CLEANING PROCESS FOR NOBLE METAL
INTEGRATED CIRCUIT STRUCTURES**

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BACKGROUND OF THE INVENTION

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Thin films of noble metals (Pt, Pd, Ir, Rh) have become technologically important in integrated circuits (ICs) as electrodes for ferroelectric and high ϵ thin films in FeRAMs, DRAMs, RF and microwave MMICs, pyroelectric IR focal plane detector arrays, etc.

The absence of viable dry etching techniques for submicron patterning of these electrodes is a chronic problem that has threatened to retard or even prevent widespread use of these materials. The present dry-etching approaches utilize plasmas for reactive ion etching (RIE), are chlorine-based, and result in significant residue being left on the microelectronic device structure after the etch process has been completed.

Depending on the type of structure that is being formed by the patterning step, this post-etch residue may result in short circuiting, undesired topography or other deficiencies in the operation of the circuit element in subsequent use of the product microelectronic device. Prevention of the formation of such residues may be achieved in some instances by manipulating the reactive ion etching (RIE) process parameters, but such process manipulation results in undesirable sidewall slopes in the microelectronic device structure that effectively prevent useful submicron capacitors from being fabricated.

Alternatively, the residue resulting from RIE can be removed by wet rinsing techniques, after the etch process has been completed. Wet rinsing techniques are however generally unsatisfactory, because a significant fraction of the residue may be transported in suspension in the rinse media, allowing a small fraction of the residue solids to redeposit on the wafer, and thereby reducing device yield.

Further, in some microelectronic device structure geometries, the residue may not be removed using wet rinsing methods.

Another drawback of wet rinsing methods is the need for a separate process tool to implement the wet rinsing clean-up, which adds to the capital equipment and operating costs of the process system.

It would therefore be a significant advance in the art of integrated circuit device fabrication, in which noble metal films are formed on the device substrate as electrodes

or other structural components of the device, to provide an effective cleaning process for removing unwanted residues on the integrated circuit structure after etching or other process fabrication steps.

SUMMARY OF THE INVENTION

The present invention relates to a method for removing noble metal residue from a microelectronic device structure during the fabrication thereof, by contacting the microelectronic device structure with a gas-phase reactive halide composition, e.g., XeF_2 , SF_6 , Si_2F_6 , SiF_4 , or SiF_2 and /or SiF_3 radicals, for sufficient time and under sufficient conditions to at least partially remove the noble metal residue.

Such "dry clean" method of the invention effects an isotropic dry etching of the noble metal residue for removal thereof. The isotropic dry etching is carried out under low-pressure exposure of the noble metal residue to the reactive halide gas.

The reactive halide may comprise any suitable halide substituent, e.g., fluorine, bromine, chlorine, or iodine, with fluorine generally being most preferred. The reactive halide agent may itself comprise the reaction product of an initial reaction, such as the reaction of XeF_2 with silicon to form SiF_2 and/or SiF_3 radicals as the reactive halide agent. In this manner SF_6 , SiF_4 or Si_2F_6 may be used with an activation source (ion beam, electron beam, ultra violet or laser) to produce the reactive radical species.

The invention contemplates two main cleaning techniques for using the reactive halide gas as an isotropic noble metal etch agent to remove residual noble metal deposits from the microelectronic device structure.

The first technique is a batch contacting method wherein a chamber containing the microelectronic device structure is evacuated and backfilled with the reactive halide gas or a mixture of the reactive halide gas and other gas(es), either inert or reactive. After the reactive halide is allowed to react for a predetermined amount of time, the chamber is evacuated and backfilled again with fresh cleaning gas. The evacuation pressure can be less than or equal to 50 mTorr. The backfill pressure can be from about 50 mTorr to about 2 Torr, the exposure time can be from about 10 seconds to about 10 min, and the number of exposure cycles is not limited, but will depend on the amount of material to be removed.

The second technique using the reactive halide gas as an isotropic etch agent is a continuous gas flow method. In this technique, a steady state flow of the reactive halide gas, e.g., XeF_2 , SF_6 , Si_2F_6 or SiF_4 , is introduced to the chamber containing the microelectronic device structure to be cleaned. Either pure reactive halide gas or a mixture of the reactive halide and other gas(es), either inert or reactive, may be used. The partial pressure of the reactive halide gas can be from about 50 mTorr to about 2 Torr and total flow rate of the reactive halide gas can be from about 1 standard cubic centimeter per minute (sccm) to about 10 standard liters per minute (slm).

In either case of batch or continuous operation, the microelectronic device structure to be cleaned may be held at temperatures in the range of from about -50°C to about 200°C .

In the foregoing methodology, the reactive halide gas may for example comprise a XeF_2 vapor. Such vapor may be obtained from the sublimation of XeF_2 solid crystals. XeF_2 will sublime at room temperature, but may be heated to increase the rate of sublimation.

Additionally, the XeF_2 may first be reacted with elemental silicon, and the resultant reaction product used as the etching gas. It is known that XeF_2 etches silicon to produce SiF_4 , Si_2F_6 and SiF_2 and SiF_3 radicals.

The reactive halide composition may also be produced in an upstream plasma, e.g., SiF_2 and SiF_3 radicals may be formed by passing SiF_4 gas through a remote plasma.

The method of the invention is usefully employed for removal of noble metal residues comprising Ir, Rh, Pd and/or Pt, and may be utilized for cleaning hybrid electrodes comprising alloys or combinations of such metals, as well as alloys or combinations of one or more of such metals with other (non-noble) metals.

Other aspects, features and embodiments of the invention will be more fully apparent from the ensuing disclosure and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a process flow of a fabrication sequence embodying the method of the present invention, in one aspect thereof.

Figure 2 is a schematic representation of a process flow of an alternative method embodiment of the invention.

Figure 3 is a schematic representation of a process flow for yet another method embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION AND PREFERRED EMBODIMENTS THEREOF

The disclosure of U.S. Patent Application 08/966,796 filed November 10, 1997 in the names of Thomas H. Baum and Frank DiMeo, Jr. for "METHOD FOR ETCH FABRICATION OF IRIIDIUM-BASED ELECTRODE STRUCTURES," is incorporated herein by reference in its entirety.

In accordance with the method of the present invention, noble metal residue is removed from a microelectronic device structure including same, by contacting the microelectronic device structure with a gas-phase reactive halide composition, e.g., XeF_2 ,

SF₆, SiF₄, Si₂F₆, or SiF₃ and/or SiF₂ radicals for sufficient time and under sufficient conditions to at least partially remove the noble metal residue.

The method of the invention may be advantageously used to remove residue from a microelectronic device structure, subsequent to reactive ion etching of noble metal electrode films thereon, for patterning of the electrode in the fabrication of the microelectronic device, and/or following chemical mechanical polishing (CMP) of the electrode or a precursor structure therefor.

As used herein, the term "microelectronic device structure" refers to a microelectronic device or a processing step towards the formation of a structure for the microelectronic device that must be subjected to subsequent processing or treatment steps in order to fabricate the final product device.

The method of the present invention obviates the deficiencies of the prior art wet rinsing techniques that have been used to remove residues when noble metal structures are formed on the surface of a microelectronic substrate, device or precursor article.

The isotropic dry etch method of the present invention may be practiced with reactive halogenated compounds such as XeF₂ and/or other halide compositions as agents for removing extraneous noble metal residues that are present on the microelectronic device structure subsequent to forming noble metal electrodes or other integrated circuit components thereon, and reactive ion etching (RIE) and/or chemical mechanical

polishing (CMP) thereof. Alternatively, the removal agent for the noble metal residue may comprise a halogenated radical species such as SiF_2 or SiF_3 radicals, formed by prior reaction as hereinafter more fully disclosed.

As used herein, the term "noble metal" means a metal of the platinum group, viz., platinum, palladium, iridium or rhodium, as well as alloys and combinations including one or more of such metals, e.g., with other non-noble metal(s).

The invention contemplates two main cleaning techniques for using the reactive halide gas as an isotropic noble metal etch agent to remove residual noble metal deposits from the microelectronic device structure.

The first technique is a batch contacting method wherein a chamber containing the microelectronic device structure is evacuated and backfilled with the reactive halide gas or a mixture of the reactive halide gas and other gas(es), either inert or reactive. After the reactive halide is allowed to react for a predetermined amount of time, the chamber is evacuated and backfilled again with fresh cleaning gas. The evacuation pressure can be less than or equal to 50 mTorr. The backfill pressure can be from about 50 mTorr to about 2 Torr, the exposure time can be from about 10 seconds to about 10 min, and the number of exposure cycles is not limited, but will depend on the amount of material to be removed.

The second technique using the reactive halide gas as an isotropic etch agent is a continuous gas flow method. In this technique, a steady state flow of the reactive halide gas, e.g., XeF_2 , SF_6 , Si_2F_6 or SiF_4 , is introduced to the chamber containing the microelectronic device structure to be cleaned. Either pure reactive halide gas or a mixture of the reactive halide and other gas(es), either inert or reactive, may be used. The partial pressure of the reactive halide gas can be from about 50 mTorr to about 2 Torr and total flow rate of the reactive halide gas can be from about 1 standard cubic centimeter per minute (sccm) to about 10 standard liters per minute (slm).

In either case of batch or continuous operation, the microelectronic device structure to be cleaned may be held at temperatures in the range of from about -50°C to about 200°C .

The dry clean process of the present invention may be carried out at any suitable process condition, including ambient temperature, low temperature and elevated temperature regimes, as well as varying pressure regimes. For example, the cleaning process may be carried out at room temperature conditions involving the sublimation of XeF_2 to generate an active cleaning agent. XeF_2 may also be first reacted with another compound, such as ^{as a} ~~silicon~~ ^{silicon-containing}, to generate an active cleaning agent comprising SiF_2 or SiF_3 radicals.

The time and contacting conditions for the reactive halide etch process may be readily determined by those of ordinary skill in the art. The nature and extent of the etching of the deposited noble metal-based material may be empirically determined while varying the time and/or contacting conditions (such as temperature, pressure, concentration and

partial pressure) of the etching agent to identify the process conditions producing a desired etching result.

In the dry clean of the noble metal residue to etchingly remove same from the microelectronic device structure, the etch rates of the cleaning agent can optionally be enhanced through the use of Lewis-based adducts or electron back-bonding species, e.g., carbon monoxide, trifluorophosphine, trialkylphosphines, etc. These cleaning enhancement agents accelerate the rate of etching by enhancing the volatility of the etch by-products and noble metal (halide)_x species or noble metal (halide radical)_x species.

For example, in the case of iridium and/or iridium oxide as the noble metal on the substrate, the step of contacting the iridium-based material with a cleaning gas including the xenon halide etching reagent may be carried out with a cleaning enhancement agent such as carbon monoxide to assist in the volatilization and removal of Ir(X)₁₋₆ (where X = halide) species from the iridium-based material on the substrate. Where X = chlorine, bromine, fluorine or iodine in the presence of CO serves to enhance the reactant volatility through the formation of (CO)_yIr(X)₁₋₆. These enhancement agents can be used advantageously for etching Ir in halogen-based plasmas, ion beams and in hybrid etching schemes. Corresponding use of CO or other platinum metal hexafluorides may be utilized to remove other platinum metal residues on semiconductor device structures.

In another example, in the case of iridium and/or iridium oxide as the noble metal on the substrate, the step of contacting the iridium-based material with a cleaning gas including

the xenon halide etching reagent may be carried out with a co-etchant such as SF_6 , Si_2F_6 , SiF_4 or radical species such as SiF_3 and SiF_2 to assist in the volatilization and removal of $\text{Ir}(\text{X})_{1-6}$ (where X = silicon halide complex) species from the iridium-based material on the substrate.

The etching process using the xenon halide etching agent may also be enhanced by use of inert gases. In general, ion beam-assisted, plasma-assisted or photo-assisted techniques may be employed to enhance the etching removal of the noble metal residue, as for example by decreasing the time required for removal, or increasing the extent of removal in a given time, etc..

In application to the fabrication of specific types of microelectronic device structures, the invention has illustrative utility in the fabrication of capacitor structures. There are three principal types of capacitor geometries and associated processing paths, hereafter referred to as Type 1, Type 2 and Type 3, in which the method of the present invention offers a significant economic or enabling advantage over the methods of the prior art.

Capacitor arrays in high-density memories ($> 64 \text{ Mb}$) are typically made by patterning the bottom electrode prior to deposition and patterning of the dielectric and top electrode layers. This is referred to as a Type 1 structure.

For Type 1 structures, the prior art has used a combination of mechanical liquid agitation and partial dissolution of the residue to "clean up" the noble metal residues.

The process of the present invention provides an effective alternative to such prior art wet methods for removing noble metal residues from RIE-patterned bottom electrodes.

The process of the invention is also usefully applied to patterning approaches that define the entire capacitor in one step, including RIE of the entire metal-dielectric stack (Type 2) and chemical mechanical planarization, or chemical mechanical polishing, as such operation is sometimes termed (Type 3).

In chemical mechanical planarization, capacitors are formed in recesses and excess protruding dielectric and metal is removed by polishing, as more fully described in copending U.S. Application No. 08/975,366 filed November 20, 1997 in the names of Peter C. Van Buskirk and Peter S. Kirlin for "CHEMICAL MECHANICAL POLISHING OF FeFRAM CAPACITORS," the disclosure of which hereby is incorporated herein by reference in its entirety.

Type 1 Capacitor Structures

As mentioned, this structure is used for very high-density memories, such as those with memory density > 64Mb. Parts of the capacitor are formed on the sidewalls, with potential large increases in capacitor area.

Referring to Figure 1A of the drawings, a Type 1 capacitor array is formed over an array of transistors (not shown), which are contacted preferably by conductive plugs 1. The conductive plugs are planarized on the surface of the isolation dielectric 2, or subsequent

to capacitor formation by etching vias in which conductive plugs are formed, as shown in Figure 1A.

Next, as shown in Figure 1B, the barrier layer 3 and bottom electrode 4 are deposited, using conventional methods such as CVD or sputtering. The bottom electrode is then patterned using RIE or a similar metal etch, as illustrated in Figure 1C, prior to capacitor dielectric (high ϵ , ferroelectric, etc.) deposition.

When the electrode is patterned using the predominantly physical mechanism of the impinging ions, involatile material that is sputtered from between the electrodes is redeposited on the sidewalls of the photoresist (or hard mask), and when the mask is removed, the redeposited layers remain. These redeposited features 5, sometimes characterized as “ears,” are surprisingly robust.

The dry etch cleaning method of the present invention is usefully applied in the fabrication of such Type 1 structure and may be advantageously implemented in-situ in the RIE reactor. As shown in Figure 1D, the isotropic nature of the dry clean etch effectively removes the ears that were formed by the highly anisotropic RIE process.

The result is smooth bottom electrodes 6 that will increase device yield because of the absence of sharp features which would if otherwise present serve to enhance E-fields in the capacitor dielectric. Subsequent processing of the capacitor may then proceed (not shown), comprising dielectric deposition, dielectric patterning, top electrode deposition

and patterning, and metallization post oxidizing bake step to complete the formation of the integrated circuit.

In this Type 1 application, the process of the present invention provides a significant economic advantage over prior art wet methods. As mentioned, prior art wet methods, although effective, result in significant decrease in device yield as well as decreased throughput.

Type 2 Capacitor Structures

This type of structure is illustrated in Figure 2 and is usefully employed in lower density memory arrays (<64 Mb), where the area of the capacitor allows sufficiently high capacitance or remenant polarization.

In the process flow of Figure 2, the capacitor array is formed on a planar surface of an isolation dielectric 22, over an array of transistors (not shown). The transistors in this structure are contacted by conductive plugs 21 that have been planarized using CMP or other planarization techniques that are well known in the art. The plug and dielectric structure is illustrated in Figure 2A.

In this fabrication method, the entire capacitor system of layers, including conductive barrier 23, bottom electrode 24, dielectric (high ϵ , ferroelectric, etc.) material 25 and top electrode 26 are deposited sequentially, to produce the structure shown in Figure 2B.

The capacitors are next defined using conventional microlithography and anisotropic dry etching processes, using either 2 mask levels or 1 mask level. The use of 1 mask level is the preferred embodiment to produce the structure of Figure 2C, and is currently the most widespread technique for fabricating FeRAM capacitors.

The comparative advantages of a 2 mask process are well known, and include reducing the tendency for increased leakage currents that occur when a 1 mask approach is used. A 2 mask approach patterns the top electrode (TE) and bottom electrode (BE) to different areas (the TE is smaller), thereby reducing the chance for short circuits at the electrode edge. The 2-mask approach nonetheless is less economical than the 1 mask approach.

The method of the present invention permits the 1 mask approach to be utilized advantageously without the high level of leakage susceptibility that has been characteristic of prior art products made by such mask approach.

Due to the predominantly physical nature of the reactive ion etching process, residue collects on the sides of the capacitor structure 27, making short circuiting more likely. Additionally, sharp features ("ears") may also be present on the top edges of the top electrode 28, for the same reason as discussed hereinabove in connection with the fabrication of the Type 1 structure.

The process of the present invention is employed to remove the sidewall residue and the "ears". This process step in Figure 2D removes metallic conductive residue from the

edges of the capacitor, analogous to the use of the dry cleaning method of the invention in the fabrication of the Type 1 structure as described hereinabove.

In addition to the isotropic dry clean process, a post oxidizing bake may be performed, similar to that described above for the fabrication of the Type 1 structure. The result is a capacitor structure 29 that is formed with high yield in terms of short circuiting. In addition, the capacitor structure 29 does not have protrusions from the top edges of the top electrode. Such protrusions when present complicate the subsequent isolation of the capacitor array that is required before metallization can be carried out to complete the memory circuits of the structure.

The method of the present invention is of an enabling character in application to the fabrication of the Type 2 structure, since prior art wet methods do not effectively clean nominally planar surfaces with embedded metallic contamination.

Type 3 Capacitor Structures

This fabrication technique is shown in the process flow schematically illustrated in Figure 3. Such fabrication technique may be utilized to completely avoid the need for RIE processes to pattern noble metals and complex oxide thin films, e.g., those comprising PbZrTiO_3 , SrBiTiO_3 and BaSrTiO_3 .

The Figure 3 fabrication technique can be used to fabricate either high or low-density capacitor arrays, since enhanced capacitor area can be obtained from the sidewall contribution, if the aspect ratio of the recesses (depth/width) is large enough.

Such technique can also be used to fabricate low-density memory arrays, due to the inherent economic advantages of this methodology in minimizing the patterning complexity and the number of steps.

The capacitor array in the Figure 3 fabrication method is formed on a planar surface of an isolation dielectric 32, over an array of transistors (not shown), which are contacted by the conductive plugs 31 illustrated in Figure 3A. In this fabrication technique, capacitor recesses 33 are formed in a conventional dielectric material 34 (SiO_2 or Si_3N_4 , for example).

The capacitor recesses are aligned over the conductive plugs 31, as shown in Figure 3B. The capacitor recesses 33 will correspond to self-aligned capacitors over such conductive plugs once the patterning of the capacitors is completed.

The entire capacitor system of layers is then deposited sequentially to form the structure shown in Figure 3C. The respective layers include conductive barrier 35, bottom electrode 36, dielectric (high ϵ , ferroelectric, etc.) material 37, and top electrode 38.

The individual capacitors are next defined by chemical mechanical polishing (CMP) of the entire layer system to yield the structure shown in Figure 3D. Once the structure is formed by CMP there may be significant metal contamination ³⁹ along the edges of the capacitor on the top surface (which has been planarized) that will result in short circuiting of the capacitor if not removed from the structure. Such metallic contamination is typically due to incomplete removal and smearing of noble metal electrode material during the chemical mechanical polishing operation.

The process of the present invention next is utilized to remove the conductive metallic residue, to produce the structure as shown in Figure 3E, and thereby allow the capacitors to function as intended.

In addition to the isotropic dry clean process, a post oxidizing bake may be employed to heal surface and/or subsurface damage to the dielectric (high ϵ , ferroelectric, etc.) material. Such damage may be either chemical or physical in nature. The post oxidizing bake thereby imparts optimum insulating or ferroelectric properties (depending on the material of construction) to the dielectric material.

The result is a capacitor structure 40 shown in Figure 3E that is formed with high yield (in terms of non-short circuiting device elements), in a highly economical manner. In this application (the fabrication of Type 3 structures), the process of the present invention is enabling in character, since wet cleaning methods of the prior art do not work well to clean planar surfaces with embedded metallic contamination.

Accordingly, while the invention has been described herein with reference to specific features, aspects and embodiments, it will be recognized that the invention may be widely varied, and that numerous other variations, modifications and other embodiments will readily suggest themselves to those of ordinary skill in the art. Accordingly, the ensuing claims are to be broadly construed, as encompassing all such other variations, modifications and other embodiments, within their spirit and scope.

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